UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,492	04/12/2006	Shinji Maekawa	740756-2947	3788

22204 7590 03/10/2009

NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	
MAIL DATE	**DELIVERY MODE**
03/10/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/575,492	MAEKAWA ET AL.	
	Examiner	Art Unit	
	STANETTA D. ISAAC	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27 and 29-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-17,19-27,29,30,36,37 and 39-47* is/are allowed.

6)☒ Claim(s) *18,31-35 and 38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/03/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment and RCE filed on 2/03/09. Currently, claims 1-27 and 29 and 47 are pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/03/09 has been entered

.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 2/03/09. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 18, 31-35 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al (US PGPub.2003/0083203, hereinafter referred to as "Hoshimoto") in view of Kimura et al (US PGPub 2004/0142544, hereinafter referred to as "Kimura").

Hashimoto discloses the semiconductor method as claimed. See figures 1-13, and corresponding text, where Hashimoto shows, pertaining to claim 18, a method of manufacturing a thin film transistor, comprising the steps of: forming a first liquid-repellent region by a plasma treatment on a surface for forming a gate electrode in an upper portion of the semiconductor film ([0087] and [0097-0098]); forming selectively a first lyophilic regon in the first liquid-repellent region; and forming conductive film in the first lyophilic region of the surface of the semiconductor film dropping a composition including a conductive material ([0102]).

Hashimoto shows, pertaining to claim 31, a droplet discharging method, comprising the steps of: forming a lyophilic region by irradiating selectively on an object to be treated in which a liquid-repellent region is formed with light by a light irradiation unit([0087] and [0097-0098]; ([0100])); and discharging a droplet onto the lyophilic region by a droplet discharging unit, in a treatment chamber including the droplet discharging unit and the light irradiation unit ([0102]).

Hashimoto shows, pertaining to claim 32, a droplet discharging method, using a treatment apparatus in which a first treatment chamber having a plasma unit and a dielectric, and a second treatment chamber having a droplet discharging unit and a light irradiation unit, comprising the steps of: forming a liquid-repellent region in an object to be treated by the plasma unit and the dielectric in the first treatment chamber ([0087] and [0097-0098]); transporting the object to be treated into the second treatment chamber without being exposed to the atmosphere; forming selectively a lyophilic region in the object to be treated in which a liquid-repellent region is formed by the light irradiation unit in the second treatment chamber ([0100]); and discharging a droplet onto the lyophilic region by the droplet discharging unit ([0102]).

Hashimoto shows, pertaining to claim 33, wherein the droplet discharging unit and the light irradiation unit are integrally formed ([0115]).

Hashimoto shows, pertaining to claim 34, wherein the light irradiation unit includes laser light ([0115}).

Hashimoto shows, pertaining to claim 35, wherein the composition is dropped by an ink-jetting method ([0102]).

However, Hashimoto fails to show, pertaining to claim 18, forming selectively a (first) lyophilic region in the liquid-repellent region so that the surface includes the lyophilic region and the liquid-repellent region. In addition, Hashimoto fails to show, pertaining to claim 4, wherein the plasma treatment is performed at a pressure of 100 Torr to 1000 Torr. Finally, Hashimoto fails to show, pertaining to claim 18, forming a source electrode, drain electrode and gate electrode. Hashimoto fails to show, pertaining to claim 38, wherein the first liquid-repellent region is formed by forming a CF_2 bond on the surface by plasma treatment.

Hashimoto teaches performing a plasma treatment to create a liquid repellent ([0097-0098]).

Kimura teaches, pertaining to claim 18, using laser irradiation to heat specific regions of the semiconductor film forming irradiated and non-irradiated regions, creating TFTs for driving circuits with faster switching characteristics, and TFTs for pixels that withstand high voltage (see figures 1B and 1C; [0038-0039]). In addition, Kimura teaches pertaining to claim 18, manufacturing thin film transistors that conventionally include a source electrode, drain electrode and gate electrode (figure 1E; [0046]).

1. It would have been obvious to one of ordinary skill in the art at the time of the invention to selectively form a (first) lyophilic region in the liquid-repellent region so that the surface includes the lyophilic region and the liquid-repellent region, in the method of Hashimoto, for its benefits of heating specific regions, as disclosed by the Kimura. The substitution of heating specific regions would be within the skill of one of ordinary skill in the art with the motivation of forming a strong attraction at the surface of the semiconductor film creating a smoothly uniformed crystalline surface that provides faster switching characteristics at the irradiated portions and at the non-irradiated portions an ability to withstand high voltages. Also, regarding the plasma treatment being performed at a pressure of 100 Torr to 1000 Torr, pressure are parameters of optimization (*See In re Aller, Lancey and Hall* (10 USPQ 233-237)) where one of ordinary skill in the art would be capable of producing the desired parameters based on routine experimentation, for the purpose of creating a liquid repellent region. Forming a source electrode, drain electrode and gate electrode, in the method of Hashimoto, as taught by both Hashimoto in view of Kimura, would be obvious since both references teach forming integrated

circuits known in the art where thin-film transistors would not be precluded as a known device that conventionally incorporate source electrode, drain electrode and gate electrodes to form the device. Finally, forming a liquid-repellent region by forming a CF_2 bond on the surface by plasma treatment would be obvious based on the teachings of Hashimoto performing the plasma treatment on the surface to create the liquid-repellent surface by using a fluorine based gas, such as, tetrafluoromethane (CF_4).

Allowable Subject Matter

1. Claims 1-17, 19-27, 29, 30, 36, 37 and 39-47 are allowed over the prior art of record.

2. The following is an examiner's statement of reasons for allowance: The prior art of record and to the Examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a method for forming a wiring, particularly characterized by a step of performing selectively a lyophilic treatment on the opening portion and a peripheral region of the opening portion of the surface of the insulating film to form a lyophilic region and a liquid-repellent region, as detailed in claim 1.

3. The prior art of record and to the Examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a method for forming a wiring, particularly characterized by a step of forming selectively a lyophilic region in the liquid-repellent region so that the surface of the insulating film includes the liquid-repellent region and the lyophilic region in the opening portion and a peripheral region of the opening portion, as detailed in claims 2, 3, and 9. Claims 4-8 depend from claim 3 and claims 10-13 depend from claim 9.

4. The prior art of record and to the Examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a method for manufacturing a thin film transistor, particularly characterized by a step of performing selectively a lyophilic treatment on a region of the surface of the insulating film to form a first lyophilic region so that the surface includes the first liquid-repellent region and the first lyophilic region in the opening portion and a peripheral region of the opening portion, as detailed in claim 14. Claims 21-24, depend from claim 14.

5. The prior art of record and to the Examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a method for manufacturing a thin film transistor, particularly characterized by a step of forming selectively a first lyophilic region in the first liquid-repellent region so that the surface includes the first liquid-repellent region and the first lyophilic region in the opening portion and a peripheral region of the opening portion, as detailed in claim 15.

6. The prior art of record and to the Examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a method of manufacturing a thin film transistor, particularly characterized by the step of forming a second liquid-repellent region by a plasma treatment on a surface for forming a source electrode and drain electrode; forming selectively a second lyophilic region in the second liquid repellent region, as detailed in claim 16. Claims 36, 41 and 43 depend from claim 16.

7. The prior art of record and to the Examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a method for manufacturing a thin film transistor, particularly characterized by the step of forming a second liquid-repellent

region by plasma treatment on the semiconductor film having one conductivity and gate insulating film; forming selectively a second lyophilic region in the second liquid repellent region, as detailed in claim 17. Claim 37 depend from claim 17.

8. The prior art of record and to the Examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a method for manufacturing a thin film transistor, particularly characterized by the step of forming a second liquid-repellent region by performing a plasma treatment on the gate insulating film; forming selectively a second lyophilic in the second repellent region, as detailed in claim 19. Claim 39 depend from claim 19

9. The prior art of record and to the Examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a method for manufacturing a thin film, particularly characterized by the step of forming a second liquid-repellent region by plasma treatment on the semiconductor film; forming selectively a second lyophilic region in the second repellent region, as detailed in claim 20. Claims 40, 42 and 44 depend from claim 20

10. The prior art of record and to the Examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a method of manufacturing a thin film transistor, particularly characterized by the step of forming a second liquid-repellent region in a surface of the opening portion and the interlayer insulating film by a plasma treatment on the interlayer insulating film which the opening portion is formed; forming selectively a second lyophilic region in the opening portion of the second liquid-repellent region, as detailed in claim 25. Claims 27, 29 and 30 depend from claim 25.

11. The prior art of record and to the Examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding a method of manufacturing a thin film transistor, particularly characterized by the step of forming a second film containing fluorine over the semiconductor film having one conductivity and the gate insulating film; forming selectively a second lyophilic region in the second film containing fluorine, as detailed in claim 26. Claims 45-47 depend from claim 26.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

12. Applicant's arguments filed 2/09/09 have been fully considered but they are not persuasive. In the Remarks on pages 14-19:

13. Applicant raises the clear issue as to whether Hashimoto alone or in combination with Kimura teaches of suggests forming a source electrode and a drain electrode, forming a semiconductor film over the source electrode and a drain electrode, forming a semiconductor film over the source electrode and the drain electrode, forming a first liquid-repellent region by plasma treatment on a surface for forming a gate electrode in an upper portion of the semiconductor film, forming selectively a first lyophilic region in the first liquid-repellent region, and forming the gate electrode in the first lyophilic region of the surface of the semiconductor film by dropping a composition including a conductive material. In addition, Applicant raises the clear issue as to whether Hashimoto alone or in combination with Kimura

teaches of suggests, discharging a droplet onto the lyophilic region by a droplet discharging unit, in a treatment chamber including the droplet discharging unit and the light irradiation unit. Finally, Applicant raises the clear issue as to whether Hashimoto alone or in combination with Kimura teaches or suggests, forming selectively a lyophilic region in the object to be treated in which the liquid-repellent region is formed by the light irradiation unit in the second treatment chamber so that the object to be treated includes the lyophilic region and the liquid-repellent region.

14. The Examiner takes the position that the method for manufacturing a thin film transistor, as shown by Hashimoto and the implications of Hashimoto, taken in combination with the solid teachings of Kimura, would lead to one of ordinary skill in the art to have substituted using laser irradiation to heat specific regions forming irradiated and non-irradiated regions, and manufacturing thin film transistors that conventionally include a source electrode, drain electrode and gate electrode, as taught by Kimura, for the lyophilic and liquid-repellent surface treatments of the semiconductor and conductive films in the method of Hashimoto. Specifically, Hashimoto teaches forming film patterns with conductive film wiring materials to form electrodes (gate, source and drain electrodes) for integrated circuits ([0002]), where initially a plasma treatment is performed on the surface of a substrate in order to control a desired liquid-repellent property ([0097-0099]). Next, Hashimoto teaches that when the substrate surface has a higher liquid-repellent property than what is required, a lyophilic process using irradiation is performed ([0100-0102]). Finally, Hashimoto teaches forming conductive films on the treated surface using conventional ink-jet processing that includes a droplet discharging unit and a light irradiation unit (figure 7; [0102],[0145-0148]). The only step Hashimoto fails to teach that the lyophilic

regions in the liquid-repellent region are being formed *selectively*. Kimura provides the solid teachings to realize the advantages to heating specific regions on a substrate results in a stronger attraction at the surface of the semiconductor film creating a smoothly uniformed crystalline surface that provides faster switching characteristics at the irradiated portions and at the non-irradiated portions an ability to withstand high voltages.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STANETTA D. ISAAC whose telephone number is (571)272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
February 26, 2009

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 2812